Highly Linear Low-Power Wireless RF Receiver for WSN

1.1 Base paper abstract:

This paper introduces a low-power wireless RF receiver for the wireless sensor network. The receiver has improved linearity with incorporated current-mode circuits and high-selectivity filtering. The receiver operates at the 900-MHz industrial, scientific, and medical band and is implemented in 130-nm CMOS technology. The receiver has a frequency multiplication mixer, which uses a 300-MHz clock from a local oscillator (LO). The LO is implemented using vertical delay cells to reduce power consumption. The receiver conversion gain is 40 dB and the receiver noise. The receiver's input third-order intercept point (IIP3) is −6 dBm and the total power consumption is 1.16 mW.

1.2 Enhancement of this project:

- To implement Trans-conductance LNA (Low Noise Amplifier), Mixer & Local Oscillator Baseband Filter and TIA (Trans-impedance Amplifier).
- To implement RF receiver with the help of above listed building blocks.

1.3 Proposed title:

CMOS Implementation of Low Power and High Performance RF Receiver for WSN

1.4 Proposed Abstract:

In recent technology of high level signal processing and application will have lot of complexity to transmit and receive a signals in RF (Radio frequency) based WSN. In this part early RF module will consist of separate blocks for low noise amplifier, mixer and filter with single or double conversion voltage signal processing, for this kind number block will create more critical path, due to these area complexity and power consumption will increases, and it's not performing good in accuracy. Here this proposed work will present, 900-MHz based RF receiver in one block with local oscillator, mixer, filter, LNA and TIA. This method of proposed architecture will design in Tanner EDA at 130nm and 45nm CMOS technology with perform good in area, delay and power.

1.5 Existing system:

Wireless circuits operating in the industrial, scientific, and medical (ISM) band are under focus today. This focus arises from an increased interest in the wireless sensor network (WSN) and short-range wireless devices as the Internet of Things (IoT) continues to evolve at a rapid pace. However, the growth

in the wireless communication sector and an increasing number of wirelessly connected devices cause spectrum congestion. This congestion is manipulated by moving wireless communication to other frequency bands, nonetheless, the congestion problem still exists. A review of IoT and WSN specifications shows that devices can tolerate a large noise figure (NF) however, device power consumption should be minimized to extend the battery life. This makes low power consumption a vital design target. In addition, the wireless system should have adequate linearity to overcome the increased number of blockers as the number of connected devices is increased. Moreover, designing the wireless system to operate on a wide range of frequencies would make it more cost effective.

On the other hand, WSN or IoT transceiver is typically accompanied with energy harvesting unit from multiple sources. The dependence on the energy supplied from the energy harvesting sources varies between partial dependence and full dependence with storage capability techniques to maximize the use of energy over a period of time. In case of a self-sustainable WSN node, implementing the wireless transceiver with programmability in power consumption based on the energy availability would be useful. However, the transceiver performance needs to be assessed carefully to count for system limitations.

Examining the prior art, Masuch and Delgado-Restituto and Cruz et al.Introduce low-power receivers with lower NF; however, the former achieves high linearity with low gain while the later achieves low linearity with high gain. Khan and Wentzloff present a short-range low-power wireless receiver with Gilbert active mixer-first architecture, however, the receiver suffers from high NF, which limits the receiver sensitivity and poor linearity. Balankutty et al. present an ISM band receiver, however, it suffers from high power consumption. Low-power wireless receivers with different techniques to reduce the NF and power consumption were introduced.

1.6 **Disadvantage:**

- low frequency range
- Total power Consumption is high

1.7 **Proposed system:**

In recent technology of high level signal processing and application will have lot of complexity to transmit and receive a signals in RF (Radio frequency) based WSN. In this part early RF module will consist of separate blocks for low noise amplifier, mixer and filter with single or double conversion voltage signal processing, for this kind number block will create more critical path, due to these area complexity and power consumption will increases, and it's not performing good in accuracy. Here this proposed work will present, 900-MHz based RF receiver in one block with local oscillator, mixer, filter, LNA and TIA. This method of proposed architecture will design in Tanner EDA at 130nm and 45nm CMOS technology with perform good in area, delay and power.

1.7.1 **Wireless Sensor Networks**

In the last few years wireless sensor networks (WSNs) have drawn the attention of the research community, driven by a wealth of theoretical and practical challenges. This progressive research in WSNs explored various new applications enabled by larger scale networks of sensor nodes capable of sensing information from the environment, process the sensed data and transmits it to the remote location . WSNs are mostly used in, low bandwidth and delay tolerant, applications ranging from civil and military to environmental and healthcare monitoring. WSNs as shown in Fig.1 generally consist of one or more sinks (or base stations) and perhaps tens or thousands of sensor nodes scattered in a physical space. With integration of information sensing, computation, and wireless communication, the sensor nodes can sense physical information, process crude information, and report them to the sink. The sink in turn queries the sensor nodes for information

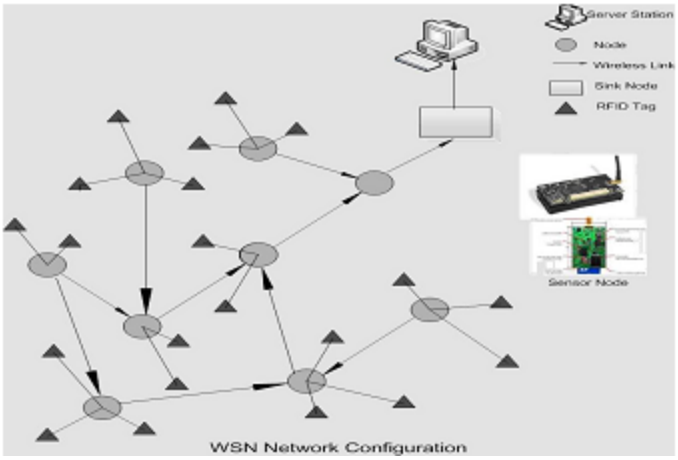
WSNs have several distinctive features like:

a) Unique network topology

b) Diverse applications

c) Unique traffic characteristics, and

d) Severe resource constraints



WSN node is comprised of low-power sensing devices, embedded processor, communication channel and power module. The embedded processor is generally used for collecting and processing the signal data taken from the sensors. Sensor element produces a measurable response to a change in the physical condition like temperature, humidity, particulate matter (e.g. CO2) etc.

The wireless communication channel provides a medium to transfer the information extracted from the sensor node to the exterior world which may be a computer network and inter-node communication. However, WSN using IEEE 802.15.4 Wireless Personal Area Network protocol (WPAN) or Bluetooth is complicated and costly. Using RFID to implement wireless communication is relatively simple and cheap Zigbee protocol can also be used for communication; alternatively the RS232 standard for wireless transmission of data can be adopted because the data rate of RFID and that of RS232 is same in terms of bits per second (bps).

1.7.2 **PROPOSED RF WIRELESS SYSTEM**

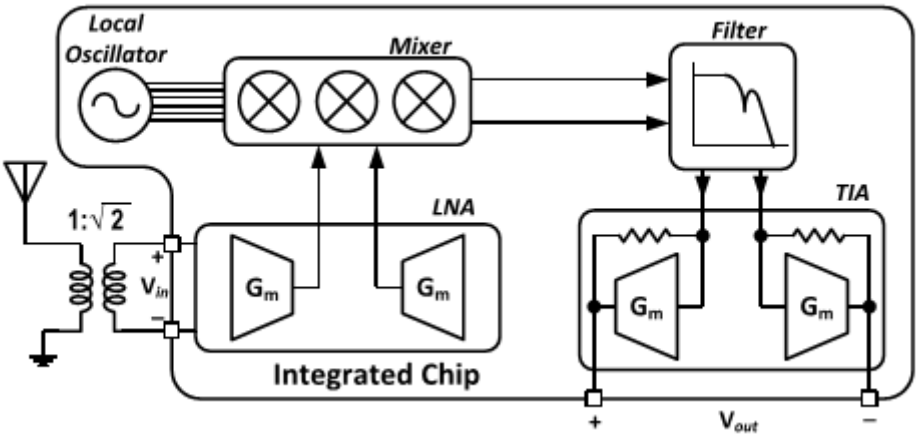


Figure 1 Proposed RF wireless receiver.

Wireless receiver architectures have been developed based on specifications and requirements. Early RF receiver architectures usually consist of separate blocks (low-noise amplifier (LNA), mixer, and filter) with voltage signal processing and either single or dual downconversion [14]. Later, more advanced receiver architectures were introduced with higher efficiency by integrating different functions in the same block with a mixture of voltage and current modes; e.g., the Blixer (a wideband balun-LNA-I/Q mixer). Recently, a mixerfirst receiver architecture was introduced as a solution to tolerate large blockers nevertheless, it suffered from high NF, which led to the introduction of a noise-canceling mixer-first architecture.

Fig. 1 shows the building blocks for the proposed receiver. The receiver operates at 900-MHz ISM band. Right after the antenna, a balun is there to convert the single-ended signal to a differential signal. The balun is followed by an LNA, which is a transconductance that transforms the RF voltage signal to an RF current signal. A passive mixer downconverts the RF current signal at 900 MHz to the baseband using a six-phase low-power ring oscillator running at 300 MHz [18]. The LO is implemented using the ring oscillator operating at 300 MHz to reduce the power consumption. After the mixer, the downconverted ac signal goes to a current-mode low-pass filter (LPF). The filter is a second-order LPF with two zeros in the stopband to sharpen the rolloff. The ac baseband signal goes from the mixer output to the filter input. Finally, there is a transimpedance amplifier (TIA) to transfer the current signal to a voltage signal and to provide the required amplification. In each block, multiple techniques are utilized to reduce the

power consumption and improve the performance while the receiver current-mode architecture improves the linearity.

Compared to mixer-first architecture, which its mixer typically operates in the voltage mode, the implemented receiver architecture operates the mixer in the current mode as the output impedance of the LNTA is high while the baseband input impedance is low. Current-mode circuit nodes are low impedance, which make the voltage swing minimal. As a result, linearity is improved.

1.7.3 **RECEIVER BUILDING BLOCKS**

1.7.3.1 Transconductance LNA

In electronics, a transimpedance amplifier, (TIA) is a current to voltage converter, almost exclusively implemented with one or more operational amplifiers. The TIA can be used to amplify the current output of Geiger–Müller tubes, photo multiplier tubes, accelerometers, photo detectors and other types of sensors to a usable voltage. Current to voltage converters are used with sensors that have a current response that is more linear than the voltage response. This is the case with photodiodes where it is not uncommon for the current response to have better than 1% nonlinearity over a wide range of light input. The transimpedance amplifier presents a low impedance to the photodiode and isolates it from the output voltage of the operational amplifier. In its simplest form a transimpedance amplifier has just a large valued feedback resistor, R_f. The gain of the amplifier is set by this resistor and because the amplifier is in an inverting configuration, has a value of $-R_f$. There are several different configurations of transimpedance amplifiers, each suited to a particular application. The one factor they all have in common is the requirement to convert the low-level current of a sensor to a voltage. The gain, bandwidth, as well as current and voltage offsets change with different types of sensors, requiring different configurations of transimpedance amplifiers.

The transconductance LNA has two roles: first, it has to convert the input voltage signal to an output current signal while introducing minimum noise. Second, it should provide input matching. As a survey for the prior art, Fig. 2 compares the transconductance LNA topologies [19], [20]. Common-source LNA is shown in Fig. 2(a). It provides reasonable transconductance while it does not provide input matching. Common-source LNA with inductive degeneration is shown in Fig. 2(b). Its Gm does not depend on transistor transconductance while it provides narrowband matching. Fig. 2(c) shows the single-ended

common-gate LNA. It provides wideband matching; however, the transistor gm should be large enough to provide the matching. Fig. 2(d) shows the cross-coupled differential common-gate LNA [21]. It provides wideband matching and the cross-coupling boosts the transistors gm. The drawback of a common-gate LNA is that it requires a large current to provide input matching. As a solution, Fig. 3 shows the basic concept of the proposed transconductance LNA. Unlike [21], complementary CMOS transistors (M2 and M3) are used to provide input matching. Both transistors have the input voltage (negative input voltage) applied at the gate (source) of the transistor to boost the transconductance by a factor of two. Additionally, M1 and M4 are added to increase the total transconductance. Current i1 is given by

$$i1 = gm1vin + 2 \times gm2vin \quad (1)$$

while i2 is given by

$$i2 = gm4vin + 2 \times gm3vin. \quad (2)$$

The output currents can be summed together and the total output current will be

$$iout = i1 + i2 = (gm1 + 2gm2 + 2gm3 + gm4)vin. \quad (3)$$

Assuming, gm1 = gm3 = gmn and gm2 = gm4 = gmp,

The total transconductance is given by

$$Gm = iout / vin = 3(gmn + gmp). \quad (4)$$

The input current is given by

$$iin = 2(gmn + gmp)vin \quad (5)$$

and the input impedance becomes

$$Zin = vin / iin = 1 / 2(gmn + gmp) . \quad (6)$$

To provide matching, the following condition should be satisfied:

$$RS = Zin = 1 / 2(gmn + gmp) \quad (7)$$

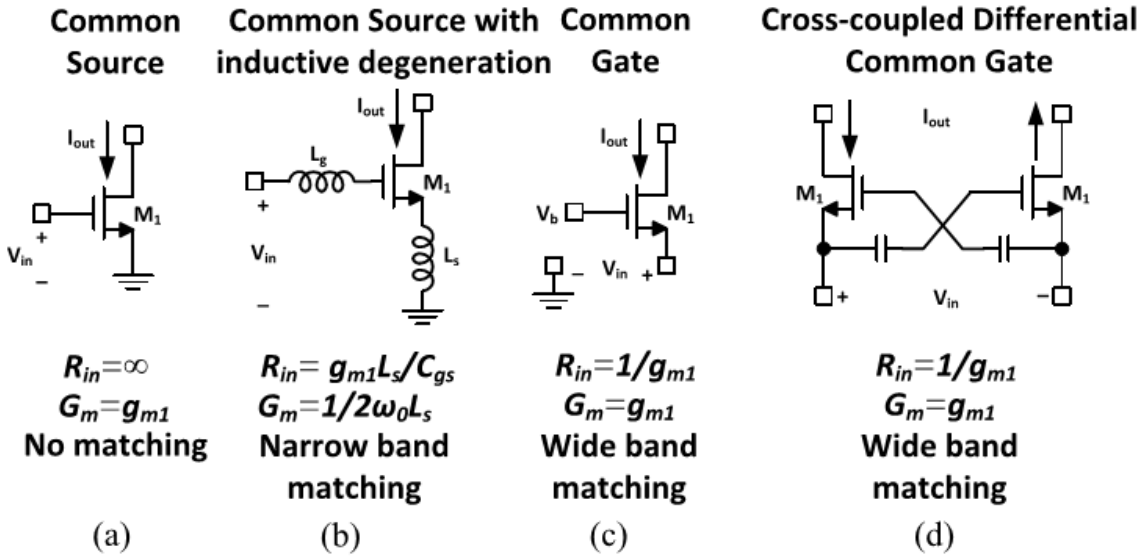


Figure 2 Transconductance LNA topologies. (a) Common source. (b) Common source with inductive degeneration. (c) Single-ended common gate. (d) Cross-coupled differential common gate.

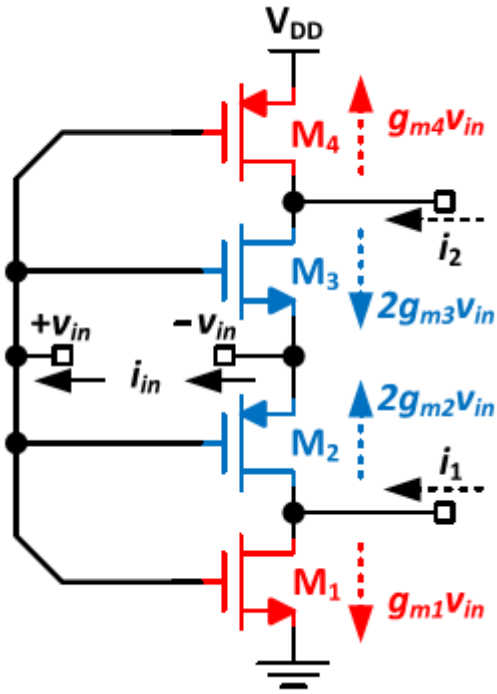


Figure 3 Proposed transconductance LNA concept.

where RS is the source impedance (antenna impedance). By stacking four transistors, matching can be achieved with lower power consumption and total transconductance can be increased by added transistors.

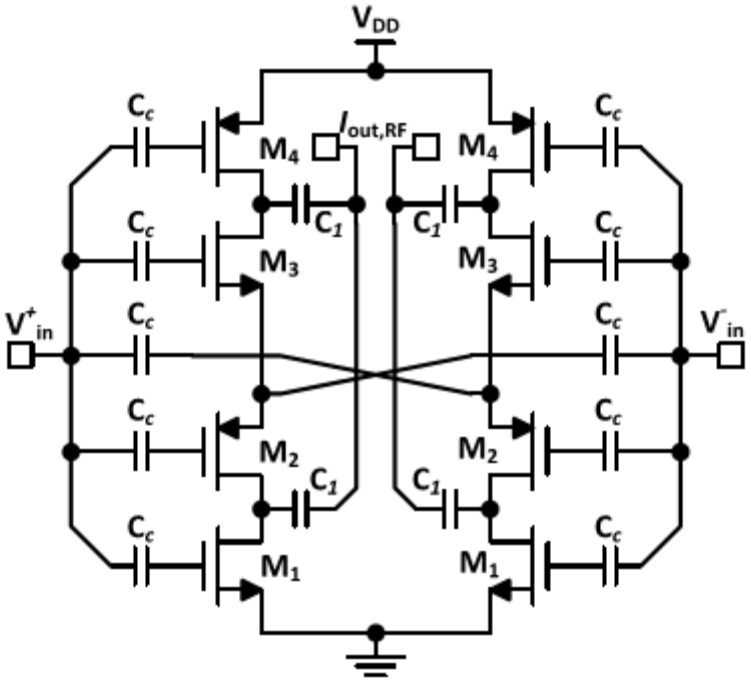


Figure 4 shows the differential and full implementation of the proposed transconductance LNA.

Capacitors are used for ac coupling at input and to combine the output currents at output. As shown in Fig. 1, the LNTA is then followed by passive mixer. Equations (1)–(7) can be used to model the proposed LNTA in Fig. 4 ideally, nevertheless, the nonidealities in the implementation seem to demand that we provide an expression for the input impedance with nonidealities. The input impedance is given as

$$Z_{\text{in,non-ideal}} = 2 \times \frac{1 + (\beta_2 + \beta_4)/sC_C}{\beta_1 + \beta_2 + \beta_3 + \beta_4} \Bigg\| \frac{1}{sC_{\text{par}}} \qquad (8)$$

where CC is the ac coupling capacitor, Cpar is the total parasitic capacitor seen at the LNTA input from all transistors gate capacitance, and β1 is given by

$$\beta_1 = \frac{r_{ds2}}{2Z_{\text{mix}} \parallel r_{ds1} + r_{ds2}} g_{m2} + \left(\frac{r_{ds2}}{2Z_{\text{mix}} \parallel r_{ds1} + r_{ds2}} - 1 \right) g_{m1} \tag{9}$$

where rds1 and rds2 are the drain-to-source impedance for transistors M1 and M2, respectively. Zin,mixer is the impedance seen at the mixer input. β2 is given by

$$\beta_2 = \frac{r_{ds2}}{2Z_{\text{mix}} \parallel r_{ds1} + r_{ds2}} (g_{m2} + 1/r_{ds2}). \tag{10}$$

β3 is given by

$$\beta_3 = \frac{r_{ds3}}{2Z_{\text{mix}} \parallel r_{ds4} + r_{ds3}} g_{m3} + \left(\frac{r_{ds3}}{2Z_{\text{mix}} \parallel r_{ds4} + r_{ds3}} - 1 \right) g_{m4} \tag{11}$$

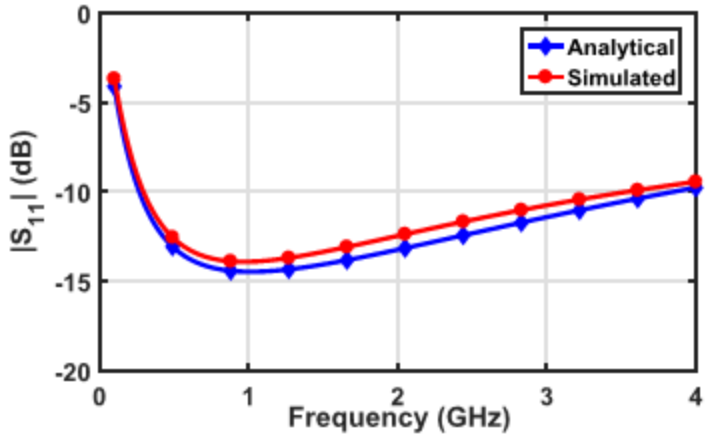


Figure 5 Simulated and analytical |S11| for transconductance LNA

where rds3 and rds4 are the drain-to-source impedance for transistors M3 and M4, respectively. β4 is given by

$$\beta_4 = \frac{r_{ds3}}{2Z_{\text{mix}} \parallel r_{ds4} + r_{ds3}}(g_{m3} + 1/r_{ds3}). \qquad (12)$$

From (8), we can see that the transconductance used for matching (gm2 and gm3) is slightly reduced by gm1 and gm4 with a factor due to nonidealities. That would result in an increase in Zin,non-ideal and higher power consumption is needed for better matching. For the transconductance LNA, S11 is given by

$$S_{11} = \frac{Z_{\text{in,non-ideal}} - R_S}{Z_{\text{in,non-ideal}} + R_S}. \qquad (13)$$

To verify (8) and (13), analytical |S11| is compared with simulated one in Fig. 5. This figure shows a good agreement between simulation and analysis.

For the noise calculation, the total output noise from the circuit is given by

$$\begin{aligned}\overline{i_{n,\text{out}}^2} &= \overline{i_{n,M1}^2} + \overline{i_{n,M2}^2}/4 + \overline{i_{n,M3}^2}/4 + \overline{i_{n,M4}^2} \\ &= 4kT\gamma\,(g_{m1} + g_{m2}/4 + g_{m3}/4 + g_{m4}) \qquad (14)\end{aligned}$$

where k is Boltzmann's constant, T is the temperature in Kelvin degrees, and γ is the excess noise factor. The noise from M1 and M4 appears directly at the output while part of noise current from M2 and M3 go to the output. The output noise from RS is given by

$$\overline{i_{n,R_S}^2} = 2 \times kTR_S \times (g_{m1} + 2g_{m2} + 2g_{m3} + g_{m4})^2. \qquad (15)$$

The NF is given by

$$\text{NF} = 1 + \frac{2\gamma}{R_S}\frac{g_{m1} + g_{m2}/4 + g_{m3}/4 + g_{m4}}{(g_{m1} + 2g_{m2} + 2g_{m3} + g_{m4})^2}. \qquad (16)$$

If gm1 = gm2 = gm3 = gm4 = gm and using matching condition RS = 1/4gm, NF will be simplified to NF ≈ 1 + (5/9)γ . From (16), NF = 4.8 dB while NF = 4 dB from simulation. NF from the LNTA will affect the total

receiver NF along the NF from the mixer, baseband filter, and TIA. In this design, we have stacked four transistors to share the bias current and save the power consumption from nominal supply voltage (1.5 V). The transistors are biased in subthreshold, consequently, the linearity is affected. A tradeoff between power and linearity takes place. The dc current in the stack is controlled by a current mirror circuit connected to M1. In dc, M2 and M4 are diode-connected transistors with large resistance. M3 is biased via large resistance.

1.7.3.2 Mixer and LO Generation

1.7.3.2.1 Local oscillator

In electronics, a local oscillator (LO) is an electronic oscillator used with a mixer to change the frequency of a signal. This frequency conversion process, also called heterodyning, produces the sum and difference frequencies from the frequency of the local oscillator and frequency of the input signal. Processing a signal at a fixed frequency gives a radio receiver improved performance. In many receivers, the function of local oscillator and mixer is combined in one stage called a "converter" - this reduces the space, cost, and power consumption by combining both functions into one active device.

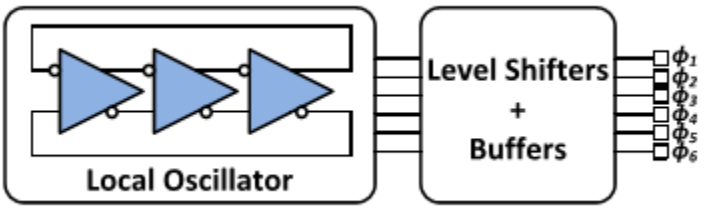


Figure 6 Block diagram for clock generation.

1.7.3.2.2 Mixer

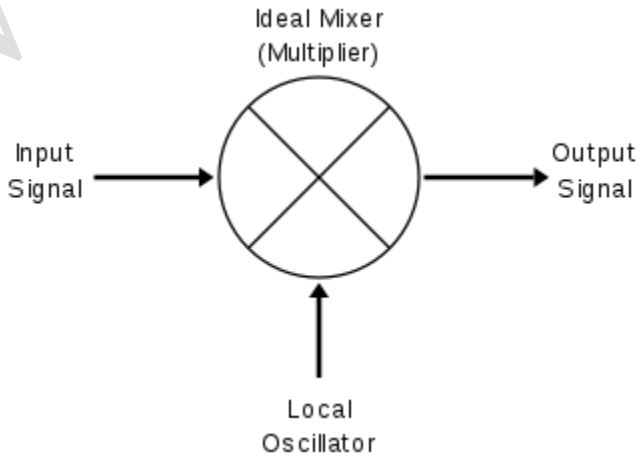
In electronics, a mixer, or frequency mixer, is a nonlinear electrical circuit that creates new frequencies from two signals applied to it. In its most common application, two signals are applied to a mixer, and it produces new signals at the sum and difference of the original frequencies. Other frequency components may also be produced in a practical frequency mixer.

Mixers are widely used to shift signals from one frequency range to another, a process known as heterodyning, for convenience in transmission or further signal processing. For example, a key component of a super heterodyne receiver is a mixer used to move received signals to a common intermediate frequency. Frequency mixers are also used to modulate a carrier signal in radio transmitters.

The essential characteristic of a mixer is that it produces a component in its output which is the product of the two input signals. A device that has a non-linear (e.g. exponential) characteristic can act as a mixer. Passive mixers use one or more diodes and rely on their non-linear relation between voltage and current to provide the multiplying element. In a passive mixer, the desired output signal is always of lower power than the input signals.

Active mixers use an amplifying device (such as a transistor or vacuum tube) to increase the strength of the product signal. Active mixers improve isolation between the ports, but may have higher noise and more power consumption. An active mixer can be less tolerant of overload.

Mixers may be built of discrete components, may be part of integrated circuits, or can be delivered as hybrid modules.



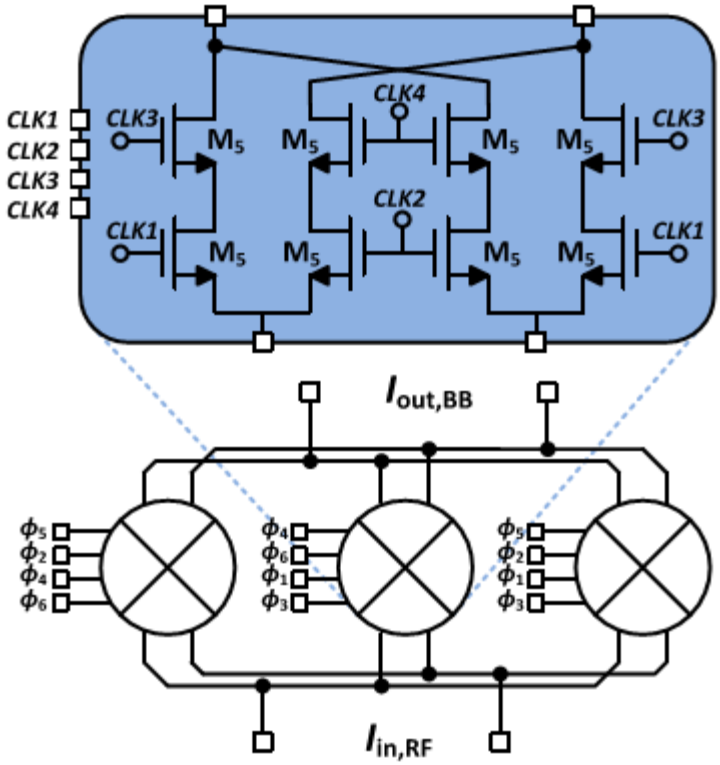


Figure 7 Proposed mixer schematic.

Fig. 6 shows the block diagram for the clock generation. It employs the ring oscillator proposed. The ring oscillator is based on vertical delay cells to recycle the charge and reduce the power consumption. The oscillator consists of three differential stages. The oscillator operates at 300 MHz to reduce the power consumption and produces six phases shifted TLO/6 apart. In order to down convert the signal at 900 MHz with 300 MHz, two steps should be implemented:

Oscillator phases should be combined to generate three times higher clock phases and the mixer should switch every TLO/3. The later can be implemented by having three mixers in parallel with one mixer active every TLO/3. The former can be implemented by AND process between the six clock phases. The full schematic of the mixer is shown in Fig. 7. It consists of three double balanced mixers in parallel. Each mixer is active every TLO so the RF input signal sees one active mixer every TLO/3. The mixer uses the six clock phases from the oscillator ϕ1 : ϕ6. Each mixer, enlarged at the top of Fig. 7, has four clock inputs.

The mixer has two transistors in series to perform the AND process between the oscillator phases without consuming power.

for a mixer with a 50% duty cycle clock is AI, mixer = 2/π. The mixer input impedance including the frequency translated impedance is given by

$$Zin,mixer(\omega) \sim= 4RSW+ 4\ \pi 2\ [Zin,F\ (\omega-\omega LO)+Zin,F\ (\omega+\omega LO)] \quad (17)$$

where RSW is the switch resistance of transistor M5 and Zin,F(ω) is the baseband input impedance of the filter.

1.7.3.3 Baseband filtering

It is sometimes desirable to have circuits capable of selectively filtering one frequency or range of frequencies out of a mix of different frequencies in a circuit. A circuit designed to perform this frequency selection is called a filter circuit, or simply a filter. A common need for filter circuits is in high-performance stereo systems, where certain ranges of audio frequencies need to be amplified or suppressed for best sound quality and power efficiency. You may be familiar with equalizers, which allow the amplitudes of several frequency ranges to be adjusted to suit the listener's taste and acoustic properties of the listening area. You may also be familiar with crossover networks, which block certain ranges of frequencies from reaching speakers. A tweeter (high-frequency speaker) is inefficient at reproducing low-frequency signals such as drum beats, so a crossover circuit is connected between the tweeter and the stereo's output terminals to block low-frequency signals, only passing high-frequency signals to the speaker's connection terminals. This gives better audio system efficiency and thus better performance. Both equalizers and crossover networks are examples of filters, designed to accomplish filtering of certain frequencies.

Another practical application of filter circuits is in the "conditioning" of non-sinusoidal voltage waveform in power circuits. Some electronic devices are sensitive to the presence of harmonics in the power supply voltage, and so require power conditioning for proper operation. If a distorted sine-wave voltage behaves like a series of harmonic waveforms added to the fundamental frequency, then it

should be possible to construct a filter circuit that only allows the fundamental waveform frequency to pass through, blocking all (higher-frequency) harmonics.

We will be studying the design of several elementary filter circuits in this lesson. To reduce the load of math on the reader, I will make extensive use of spice as an analysis tool, displaying Bode plots (amplitude versus frequency) for the various kinds of filters. Bear in mind, though, that these circuits can be analyzed over several points of frequency by repeated series parallel analysis, much like the previous example with two sources (60 and 90 Hz), if the student is willing to invest a lot of time working and re-working circuit calculations for each frequency.

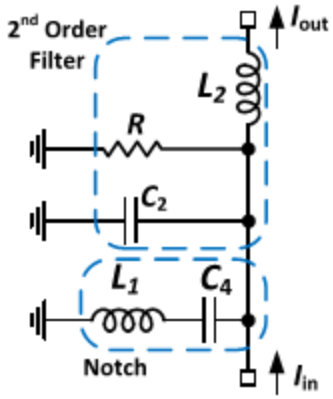


Figure 8 Filter model

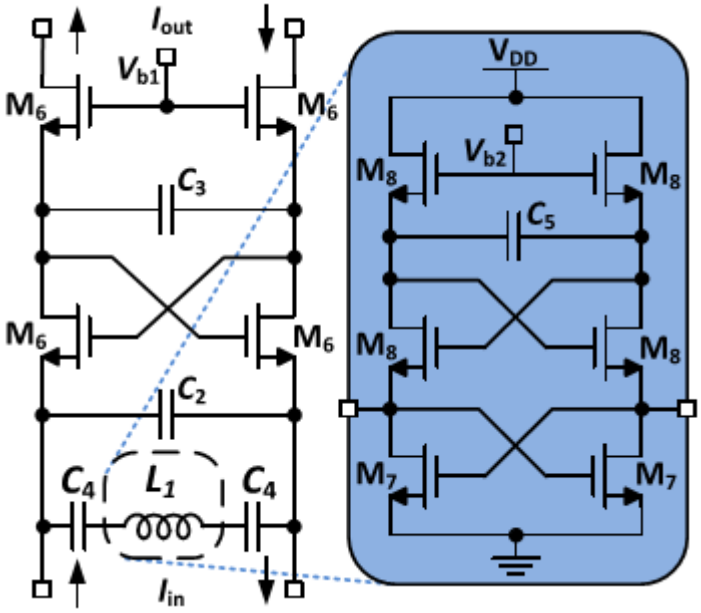


Figure 9 Filter schematic.

The filter has an important role in the receiver design to provide the selectivity for the signal of interest and to limit the noise. There is always a tradeoff in the design of the filter. Power, linearity, noise, and selectivity are the key parameters in designing the baseband filter. In this receiver, the used filter is a second-order low-pass current-mode filter. To sharpen the filter selectivity, shunt series resonance is added at the input of the filter to provide notch in the stop band. The model of the filter is shown in Fig. 8. The second-order LPF is implemented with L2, R, and C2 while the notch is implemented with L1 and C4. For implementation, Fig. 9 shows the implementation of the filter. Active inductor [26] is used to emulate inductance. The inductor for the shunt series resonance is enlarged in the right side of Fig. 9. M8 transistors and C5 are used to emulate inductor L1 while M7 provides negative resistance to cancel the inductor resistance. Inductors L1 and L2 are given by L1 = 4C5/g2 m8 and L2 = 4C3/g2 m6, respectively. In simulation, the lowest Q for L1 in bandwidth of 30% of notch frequency is 27. The power consumption for L1 is 185 µW. Adding L1 does not degrade receiver in-band noise performance as the noise products from L1 active transistors appear at baseband output only at the vicinity of notch frequency. The total transfer function for the filter is given in (18), as shown at the bottom of the next page. It is calculated under the condition that gm7 = gm8. The single side filter input impedance is given by

The power per pole is 60 µW

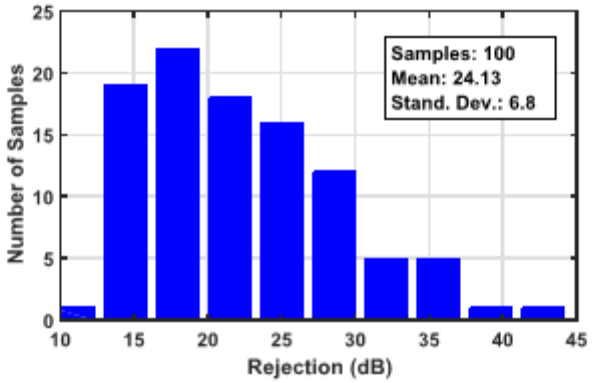


Figure 10 Monte Carlo simulation for notch rejection.

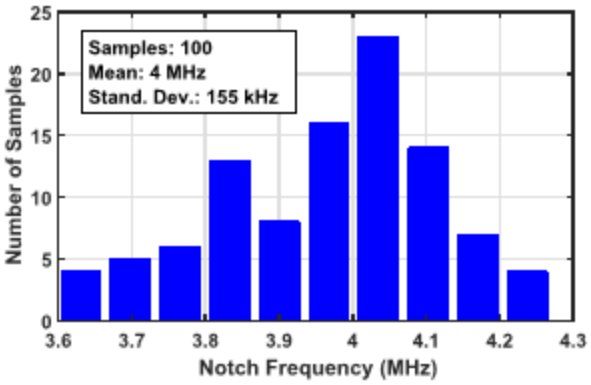


Figure 11 Monte Carlo simulation for notch frequency.

Active inductor is sensitive to process, voltage, and temperature and bias variations, especially when the active inductor is used to implement a notch in the stop band. In order to study the impact of those variations, Fig. 10 shows the Monte Carlo simulation for the notch rejection. In the simulation, process and mismatch variations are applied with 100 samples. While the rejection varies with process and mismatch, the rejection is still good for most of the samples. Fig. 11 the Monte Carlo simulation for the frequency of the notch. The plot shows that the notch frequency does not have large variation (standard deviation = 155 kHz) with the process and mismatch variations.

1.7.3.4 Transimpidence amplifier

In electronics, a transimpedance amplifier, (TIA) is a current to voltage converter, almost exclusively implemented with one or more operational amplifiers. The TIA can be used to amplify the current output of Geiger–Müller tubes, photo multiplier tubes, accelerometers, photo detectors and other types of sensors to a usable voltage. Current to voltage converters are used with sensors that have a current response that is more linear than the voltage response. This is the case with photodiodes where it is not uncommon for the current response to have better than 1% nonlinearity over a wide range of light input. The transimpedance amplifier presents a low impedance to the photodiode and isolates it from the output voltage of the operational amplifier. In its simplest form a transimpedance amplifier has just a large valued feedback resistor, R_f. The gain of the amplifier is set by this resistor and because the amplifier is in an inverting configuration, has a value of $-R_f$. There are several different configurations of transimpedance amplifiers, each suited to a particular application. The one factor they all have in common is the requirement to convert the low-level current of a sensor to a voltage. The gain, bandwidth, as well as current and voltage offsets change with different types of sensors, requiring different configurations of transimpedance amplifiers.

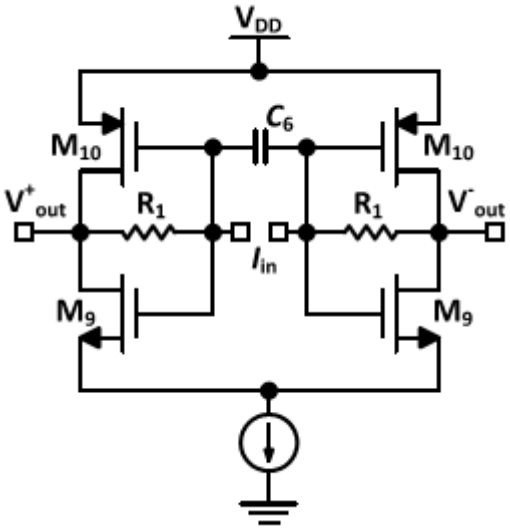


Figure 12 TIA schematic.

The TIA role is to convert the current signal to voltage signal. The schematic of the TIA is shown in Fig. 12. It consists of a complementary CMOS to reduce the power consumption. Capacitor (C6) is added to improve the filtering. The transimpedance transfer function is given by

$$A_{T,\mathrm{TIA}} = \frac{v_{\mathrm{out}}}{i_{\mathrm{in}}} = -\frac{(g_{m9} + g_{m10})R_1 - 1}{g_{m9} + g_{m10} + 2C_6 s}. \qquad (20)$$

The transfer function has pole at (gm9 + gm10)/2C6

The total receiver voltage gain is given by

$$A_{\mathrm{Rx}} = G_{m,\mathrm{LNTA}} \times \frac{Z_{o,\mathrm{LNTA}}}{Z_{o,\mathrm{LNTA}} + Z_{\mathrm{in,mixer}}} \times A_{I,\mathrm{mixer}} \times A_{I,\mathrm{filter}} \times \frac{Z_{o,\mathrm{filter}}}{Z_{o,\mathrm{filter}} + Z_{\mathrm{in,TIA}}} \times A_{T,\mathrm{TIA}} \qquad (21)$$

where Gm,LNTA is the LNTA transconductance, Zo,LNTA is the output impedance of the LNTA, Zo,filter is the output impedance of the filter, and Zin,TIA is the input impedance of the TIA

1.8 **Advantage**

- low-power highly linear wireless receiver.
- High frequency range.
- Improved linearity.
- Total power consumption is low.

Literature survey:

- "A 1.1-mW-RX-81.4-dBm sensitivity CMOS transceiver for bluetooth low energy," J. Masuch and M. Delgado-Restituto,IEEE Trans. Microw.Theory Techn. This paper presents a fully integrated low-power 130-nm CMOS transceiver tailored to the Bluetooth low energy (BLE) standard. The receiver employs a passive front-end zero-IF architecture, which is directly driven by a quadrature voltage-controlled oscillator (QVCO) without any buffering stage. The QVCO, embedded in a fractional-N phase-locked loop (PLL), employs a passive RC network to cancel the parasitic magnetic coupling between the two cores so as to keep the quadrature phase error below 1.5°. The PLL exhibits a high loop bandwidth of 1 MHz to sufficiently reduce the frequency pulling effects due to close-by interferers. The transmitter uses a direct-modulation Gaussian frequency-shift keying scheme in which small PMOS-based cells modulate the output signal of one of the cores of the QVCO. In the baseband section, the transceiver employs a 4-bit phase-domain ADC based on novel linear-combiner topology to generate the required phase rotations. The proposed combiner operates in current domain and does not employ resistors, leading to a power- and area-efficient demodulator implementation. The complete receiver achieves a sensitivity of - 81.4 dBm and fulfills the BLE requirements on interference blocking. It consumes 1.1 mW from a 1.0-V supply and has a similar power efficiency as recent super-regenerative receivers that are much more susceptible to interferers. The transmitter delivers 1.6-dBm output power to a differential 100 Ω and consumes 5.9 mW, which implies a total efficiency of 24.5%

- "Wireless sensor networks with energy harvesting technologies: A game-theoretic approach to optimal energy management," IEEE Wireless Commun. D. Niyato, E. Hossain, M. M. Rashid, and V. K. Bhargava, Energy harvesting technologies are required

for autonomous sensor networks for which using a power source from a fixed utility or manual battery recharging is infeasible. An energy harvesting device (e.g., a solar cell) converts different forms of environmental energy into electricity to be supplied to a sensor node. However, since it can produce energy only at a limited rate, energy saving mechanisms play an important role to reduce energy consumption in a sensor node. In this article we present an overview of the different energy harvesting technologies and the energy saving mechanisms for wireless sensor networks. The related research issues on energy efficiency for sensor networks using energy harvesting technology are then discussed. To this end, we present an optimal energy management policy for a solar-powered sensor node that uses a sleep and wakeup strategy for energy conservation. The problem of determining the sleep and wakeup probabilities is formulated as a bargaining game. The Nash equilibrium is used as the solution of this game.

- "A switched capacitor energy harvester based on a single-cycle criterion for MPPT to eliminate storage capacitor," X. Liu, K. Ravichandran, and E. Sánchez-Sinencio, IEEE Trans,Feb. 2018. A single-cycle criterion maximum power point tracking (MPPT) technique is proposed to eliminate the need for bulky on-chip capacitors in the energy harvesting system for Internet of Everything (IoE). The conventional time-domain MPPT features ultra-low power consumption; however, it also requires a nanofarad-level capacitor for fine time resolution. The proposed maximum power monitoring does not rely on the time-domain, but on logic criterion that can be simply determined by a finite-state machine where the maximum photovoltaic (PV) power occurs at minimum conversion ratio and maximum switching frequency. Single-cycle is used as the criterion to determine the magnitude of the output power. Practical concerns, such as self-startup and self-sustaining capabilities are here addressed by proper design of the reconfigurable switched capacitor power converter. A hysteretic control not only regulates the output, but also avoids the loading condition in IoE applications. This harvester simultaneously addresses the challenges including self-startup, self-sustaining capability, and regulated output without using a storage capacitor. Compared with various PV cells, the power conversion efficiency has a peak value of 72%, which remains above 60% for a wide harvesting voltage and power range. The chip area is as small as 0.552 mm^2

- “13.4 A 6.3 mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network,” T. Sano et al., in IEEE ISSCC Dig. Tech. Papers, Feb. 2015 In previous research, solutions to the requirements for BLE have been widely discussed such as using the sliding IF (SIF) architecture in the RX [1,2] and a Class-D amplifier with HD2 calibration [4] in the TX to achieve lower current consumption. The SIF architecture, however, involves RF image blocking violation without exception rule or the use of additional off-chip filters. In the TX, meanwhile, the calibration incurs a weakness in terms of the offset issue. Moreover, there is no approach to achieve "zero" external components for the RF port. In this paper, a BLE transceiver, with a reconfigurable filter, embedded into an on-chip matching network without any external components, is presented.

- “8.1 nJ/b 2.4 GHz short-range communication receiver in 65 nm CMOS,” O. U. Khan and D. D. Wentzloff, IEEE Trans, Jul. 2015. An 8.1 nJ/bit 2.4 GHz receiver with integrated digital baseband supporting O-QPSK DSSS modulation compliant with the IEEE 802.15.4 standard is presented that targets short-range, Internet of Things applications (IoTs). The sensitivity of a wireless communication receiver in general trades with power consumption. This receiver exploits this tradeoff to achieve a total power consumption of 2.02 mW including ADCs and digital baseband processing, at a sensitivity of -52.5 dBm at 250 Kbps. The energy-efficiency of the radio frequency (RF) front-end alone is nearly 2x better than the prior art. The receiver was fabricated in 65 nm CMOS with an area of 0.86 mm^2.

- “A 0.6-V zeroIF/low-IF receiver with integrated fractional-N synthesizer for 2.4-GHz ISM-band applications,” A. Balankutty, S.-A. Yu, Y. Feng, and P. R. Kinget, IEEE J.,Mar. 2010. Supply voltage reduction with process scaling has made the design of analog, RF and mixed mode circuits increasingly difficult. In this paper, we present the design of an ultra-low voltage, low power and highly integrated dual-mode receiver for 2.4-GHz ISM-band applications. The receiver operates reliably from 0.55-0.65 V and is compatible with commercial standards such as Bluetooth and ZigBee. We discuss the design challenges at low voltage supplies such as limited f_T for transistors and higher nonlinearities due to limited available signal swing, and present the architectural and circuit level design techniques used to overcome these challenges. The highly integrated

receiver prototype chip contains RF front-end circuits, analog baseband circuits and the RF frequency synthesizer and was fabricated in a standard digital 90-nm CMOS process; it achieves a gain of 67 dB, noise figure of 16 dB, IIP_3 of -10.5 dBm, synthesizer phase noise of - 127 dBc/Hz at 3-MHz offset, consumes 32.5 mW from 0.6 V and occupies an active area of 1.7 mm^2.

Reference:

[1] J. Masuch and M. Delgado-Restituto, "A 1.1-mW-RX-81.4-dBm sensitivity CMOS transceiver for bluetooth low energy," IEEE Trans. Microw. Theory Techn., vol. 61, no. 4, pp. 1660–1673, Apr. 2013.

[2] D. Niyato, E. Hossain, M. M. Rashid, and V. K. Bhargava, "Wireless sensor networks with energy harvesting technologies: A game-theoretic approach to optimal energy management," IEEE Wireless Commun., vol. 14, no. 4, pp. 90–96, Aug. 2007.

[3] X. Liu, K. Ravichandran, and E. Sánchez-Sinencio, "A switched capacitor energy harvester based on a single-cycle criterion for MPPT to eliminate storage capacitor," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 2, pp. 793–803, Feb. 2018.

[4] H. Cruz, H.-Y. Huang, S.-Y. Lee, and C.-H. Luo, "A 1.3 mW low-IF, current-reuse, and current-bleeding RF front-end for the MICS band with sensitivity of −97 dbm," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 6, pp. 1627–1636, Jun. 2015.

[5] O. U. Khan and D. D. Wentzloff, "8.1 nJ/b 2.4 GHz short-range communication receiver in 65 nm CMOS," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 7, pp. 1854–1862, Jul. 2015.

[6] A. Balankutty, S.-A. Yu, Y. Feng, and P. R. Kinget, "A 0.6-V zeroIF/low-IF receiver with integrated fractional-N synthesizer for 2.4-GHz ISM-band applications," IEEE J. Solid-State Circuits, vol. 45, no. 3, pp. 538–553, Mar. 2010.

[7] S. Lee, I. Choi, H. Kim, and B. Kim, "A sub-mW fully integrated wide-band receiver for wireless sensor network," IEEE Microw. Wireless Compon. Lett., vol. 25, no. 5, pp. 319–321, May 2015.

[8] A. Selvakumar, M. Zargham, and A. Liscidini, “A 600 µW bluetooth low-energy front-end receiver in 0.13 µm CMOS technology,” in IEEE ISSCC Dig. Tech. Papers, Feb. 2015, pp. 1–3.

[9] K. Wang, J. Koo, R. Ruby, and B. Otis, “21.7 A 1.8 mW PLL-free channelized 2.4 GHz ZigBee receiver utilizing fixed-LO temperaturecompensated FBAR resonator,” in IEEE ISSCC Dig. Tech. Papers, Feb. 2014, pp. 372–373.

[10] Z. Lin, P.-I. Mak, and R. P. Martins, “A sub-GHz multi-ISM-band ZigBee receiver using function-reuse and gain-boosted N-path techniques for IoT applications,” IEEE J. Solid-State Circuits, vol. 49, no. 12, pp. 2990–3004, Dec. 2014.

[11] T. Sano et al., “13.4 A 6.3 mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network,” in IEEE ISSCC Dig. Tech. Papers, Feb. 2015, pp. 1–3.

[12] J. Prummel et al., “13.3 A 10 mW bluetooth low-energy transceiver with on-chip matching,” in IEEE ISSCC Dig. Tech. Papers, Feb. 2015, pp. 1–3.

[13] F. Zhang, Y. Miyahara, and B. P. Otis, “Design of a 300-mV 2.4-GHz receiver using transformer-coupled techniques,” IEEE J. Solid-State Circuits, vol. 48, no. 12, pp. 3190–3205, Dec. 2013.

[14] S. Tadjpour, E. Cijvat, E. Hegazi, and A. A. Abidi, “A 900-MHz dual-conversion low-IF GSM receiver in 0.35-µm CMOS,” IEEE J. Solid-State Circuits, vol. 36, no. 12, pp. 1992–2002, Dec. 2001.

[15] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, “The blixer, a wideband balun-LNA-I/Q-mixer topology,” IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2706–2715, Dec. 2008.

[16] C. Andrews and A. C. Molnar, “A passive mixer-first receiver with digitally controlled and widely tunable RF interface,” IEEE J. Solid-State Circuits, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.

[17] D. Murphy et al., “A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications,” IEEE J. Solid-State Circuits, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.

[18] J. Zarate-Roldan et al., “0.2-nJ/b fast start-up ultralow power wireless transmitter for IoT applications,” IEEE Trans. Microw. Theory Techn., vol. 66, no. 1, pp. 259–272, Jan. 2018.

[19] B. Razavi, RF Microelectronics, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2011.

[20] H. Zhang and E. Sánchez-Sinencio, “Linearization techniques for CMOS low noise amplifiers: A tutorial,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 1, pp. 22–36, Jan. 2011.

[21] W. Zhuo et al., “A capacitor cross-coupled common-gate low-noise amplifier,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no. 12, pp. 875–879, Dec. 2005.

[22] A. Mirzaei, H. Darabi, J. C. Leete, X. Chen, K. Juan, and A. Yazdi, “Analysis and optimization of current-driven passive mixers in narrowband direct-conversion receivers,” IEEE J. Solid-State Circuits, vol. 44, no. 10, pp. 2678–2688, Oct. 2009.

[23] D. Kaczman et al., “A single–chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and +90 dBm IIP2,” IEEE J. Solid-State Circuits, vol. 44, no. 3, pp. 718–739, Mar. 2009.

[24] A. Mirzaei, H. Darabi, and D. Murphy, “Architectural evolution of integrated M-phase high-Q bandpass filters,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 52–65, Jan. 2012.

[25] H. Osman, A. Emira, A. N. Mohieldin, M. Abouzied, and A. Soliman, “On-chip high-Q bandpass filtering using N-phase current driven passive mixers,” in Proc. ECCTD, Aug. 2011, pp. 206–209.

[26] A. Pirola, A. Liscidini, and R. Castello, “Current-mode, WCDMA channel filter with in-band noise shaping,” IEEE J. Solid-State Circuits, vol. 45, no. 9, pp. 1770–1780, Sep. 2010.

[27] E. Kargaran, D. Manstretta, and R. Castello, “Design and analysis of 2.4 GHz 30 µW CMOS LNAs for wearable WSN applications,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 3, pp. 891–903, Mar. 2018.